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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,394	12/28/2001	Jum Soo Kim	054216-5016	2075
43569	7590	12/22/2006	EXAMINER	
MAYER, BROWN, ROWE & MAW LLP			NGUYEN, KHIEM D	
1909 K STREET, N.W.			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20006			2823	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	12/22/2006	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/029,394	KIM ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 16 October 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 7-15 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 7-15 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 31 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on October 16th, 2006 has been entered. A new rejection is made as set forth in this Office Action. Claims (7-15) are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 7-10 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fang (U.S. Patent 6,667,511).

In re claim 7, Fang discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation structure 127 in a semiconductor substrate 104 (col. 6, lines 50-62 and FIG. 5g);

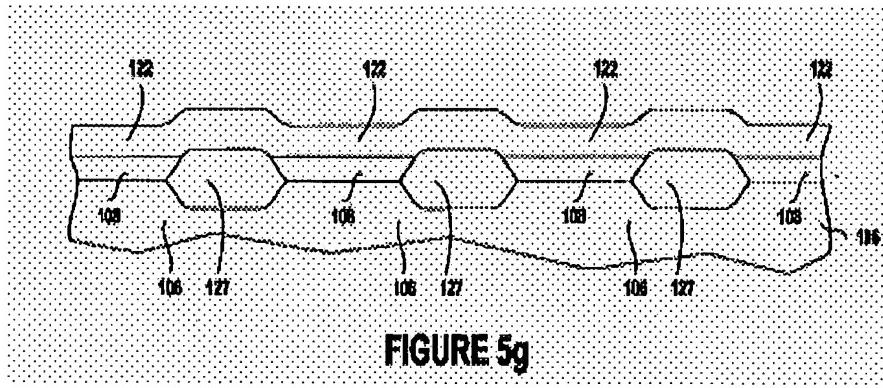
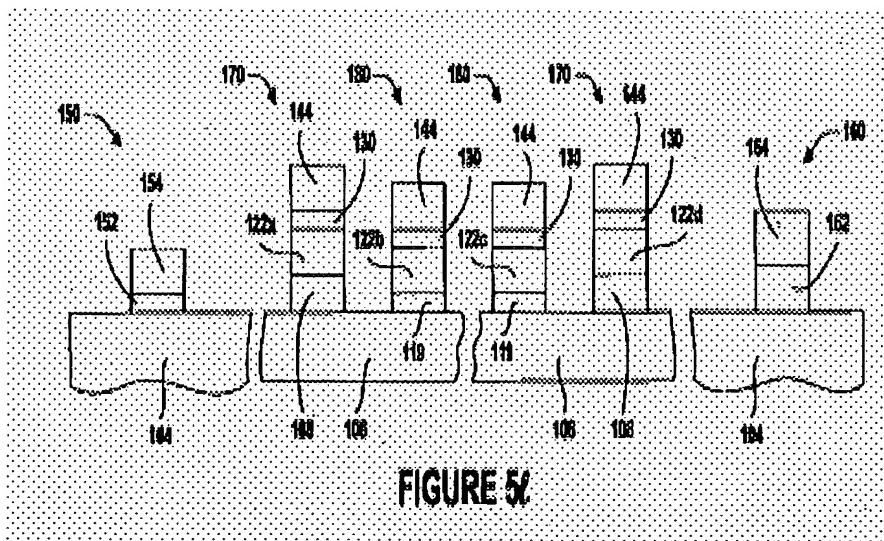


FIGURE 5g

forming a tunnel oxide layer 152 and a floating gate layer 154 in the peripheral region 150 of the semiconductor substrate 104;

a dielectric layer 130 and a control gate (poly 2) 144 over the floating gate layer (poly1) 122a in the cell region 170 and over the semiconductor substrate 104 in the peripheral region, the dielectric layer 130 including an oxide layer and a nitride layer (ONO) (col. 7, lines 31-60 and FIG. 5l); and



forming a source S and a drain D region in the semiconductor substrate 104 by performing an impurity ion implantation process (FIGS. 7a-b).

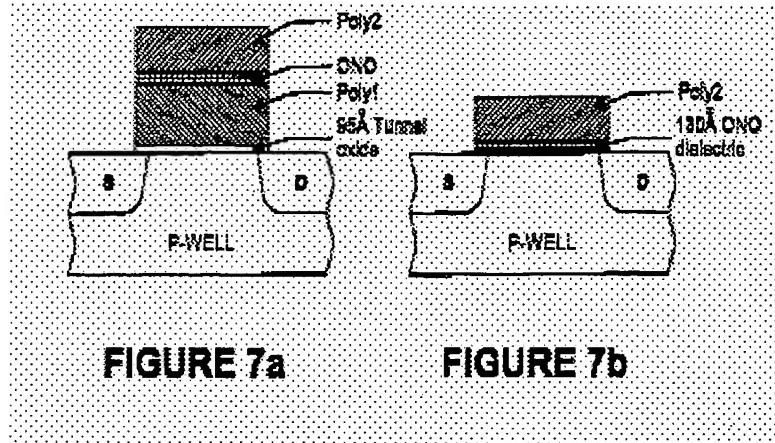


FIGURE 7a

FIGURE 7b

In re claim 8, as applied to claim 7 above, Fang discloses all claimed limitations including the limitation wherein the dielectric layer 130 is formed by stacking at least two or more layers of at least one of the oxide layer and the nitride layer (oxide-nitride-oxide, ONO layer) (col. 7, line 59).

In re claim 9, as applied to claim 7 above, Fang discloses all claimed limitations including the limitation wherein the dielectric layer 130 is formed in thickness of about 130 Angstroms (col. 10, lines 35-36).

In re claim 10, as applied to claim 7 above, Fang discloses all claimed limitations including the limitation wherein the dielectric layer 130 is formed by stacking a first oxide layer O, a nitride layer N and a second oxide layer O (ONO) (col. 7, line 59).

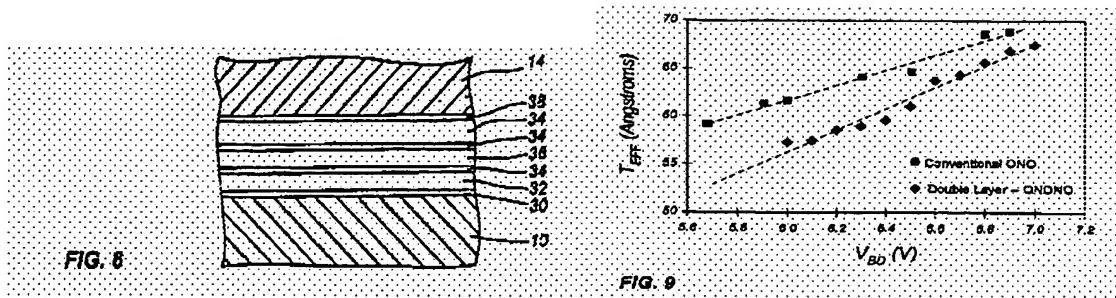
In re claim 14, as applied to claim 7 above, Fang discloses all claimed limitations including the limitation wherein the floating gate layer 122a and the control gate layer 144 is formed of polysilicon (col. 7, lines 31-60).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U.S. Patent 6,667,511) in view of Sheng et al. (U.S. Patent 5,981,404).

In re claim 11, as applied to claim 7 Paragraph 3 above, Fang discloses all the claimed limitations including a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising forming a dielectric layer 130 and a control gate (poly 2) 144 over the floating gate layer (poly1) 122a in the cell region 170 and over the semiconductor substrate 104 in the peripheral region; the dielectric layer 130 including an oxide layer and a nitride layer (oxide-nitride-oxide, ONO) (col. 7, lines 31-60 and FIG. 5l) but does not explicitly disclose that the dielectric layer is formed by stacking a first oxide layer O, a first nitride layer N, a second oxide layer O, and a second nitride layer N (ONON).

Sheng, however, discloses a insulating structures used in DRAMs or other memory devices such that the dielectric layer is formed by stacking a first oxide layer 30, a first nitride layer 32, a second oxide layer 34, and a second nitride layer 36 (ONON) between the lower doped polysilicon electrode 10 and the upper doped polysilicon electrode 14 (col. 7, lines 41-65 and FIGS. 6 and 9).



Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Fang and Sheng to enable the process of creating the dielectric layer formed by stacking a first oxide layer, a first nitride layer, a second oxide layer, and a second nitride layer of Fang to be performed and furthermore because dielectric layer having a repeated ONO structure should have a significantly reduced number of defect structures that extend directly through most or all of the dielectric layer (col. 4, lines 58-61, Sheng).

In re claim 12, as applied to claim 7 above, Fang in view of Sheng discloses all claimed limitations including the limitation wherein the dielectric layer is formed by stacking a first oxide layer 30, a first nitride layer 32, a second oxide layer 34, a second nitride layer 36, and a third oxide layer 34 (ONONO) (col. 7, lines 41-65 and FIGS. 6 and 9, Sheng).

6. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U.S. Patent 6,667,511) in view of Sheng et al. (U.S. Patent 5,981,404).

In re claim 13, Fang discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation structure 127 in a semiconductor substrate 104 (col. 6, lines 50-62 and FIG. 5g);

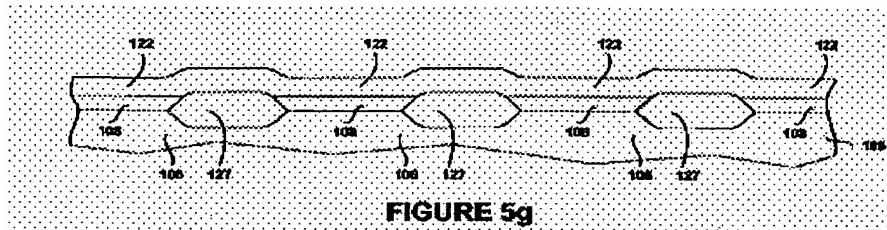


FIGURE 5g

forming a tunnel oxide layer 152 and a floating gate layer 154 in the peripheral region 150 of the semiconductor substrate 104;

a dielectric layer 130 and a control gate (poly 2) 144 over the floating gate layer (poly1) 122a in the cell region 170 and over the semiconductor substrate 104 in the peripheral region, the dielectric layer 130 including an oxide layer and a nitride layer (ONO) (col. 7, lines 31-60 and FIG. 5l); and

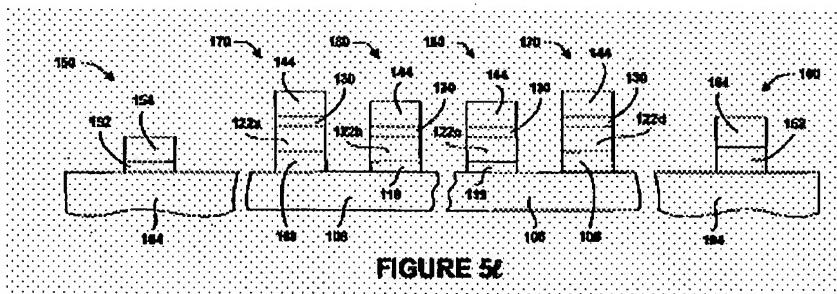


FIGURE 5l

forming a source S and a drain D region in the semiconductor substrate 104 by performing an impurity ion implantation process (FIGS. 7a-b).

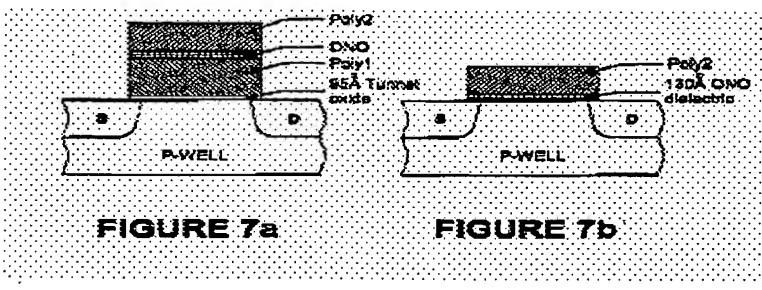


FIGURE 7a

FIGURE 7b

Fang discloses forming a dielectric layer 130 and a control gate (poly 2) 144 over the floating gate layer (poly1) 122a in the cell region 170 and over the semiconductor substrate 104 in the peripheral region, the dielectric layer 130 including an oxide layer and a nitride layer (oxide-nitride-oxide, ONO) (col. 7, lines 31-60 and FIG. 5l) but does not explicitly disclose that the dielectric layer including a first oxide layer O, a first nitride layer N, a second oxide layer O, and a second nitride layer N and a third oxide layer O (ONONO).

Sheng, however, discloses a insulating structures used in DRAMs or other memory devices such that the dielectric layer is formed by stacking a first oxide layer 30, a first nitride layer 32, a second oxide layer 34, a second nitride layer 36, and a third oxide layer (ONONO) between the lower doped polysilicon electrode 10 and the upper doped polysilicon electrode 14 (col. 7, lines 41-65 and FIGS. 6 and 9).

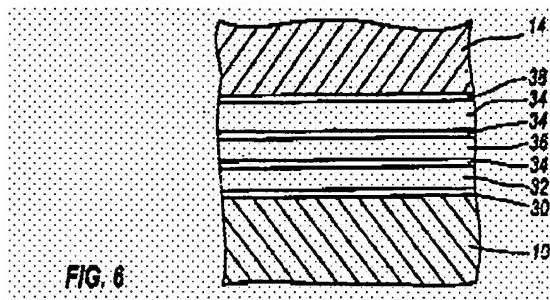


FIG. 6

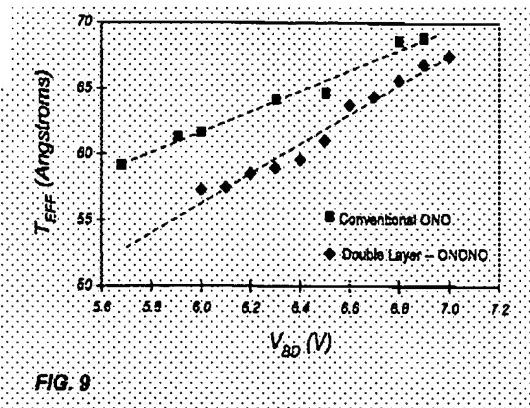


FIG. 9

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Fang and Sheng to enable the process of creating the dielectric layer including a first oxide layer, a first nitride layer, a second oxide layer, a second nitride layer, and a third oxide layer of Fang to be

performed and furthermore because dielectric layer having a repeated ONO structure should have a significantly reduced number of defect structures that extend directly through most or all of the dielectric layer (col. 4, lines 58-61, Sheng).

In re claim 15, as applied to claim 13 above, Fang discloses all claimed limitations including the limitation wherein the floating gate layer 122a and the control gate layer 144 is formed of polysilicon (col. 7, lines 31-60).

Response to Applicants' Amendment and Argument

7. Applicant's arguments with respect to claims 7-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
December 13, 2006



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